AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111 Dkt: 303.691US1

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HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES Title:

7. (Amended) A transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

[a] an edge-defined vertical floating gate separated from a first portion of the channel region by a first oxide thickness; and

at least one edge-defined vertical control gate separated from a second portion of the channel region by a second oxide thickness, wherein the at least one vertical control gate is parallel to and opposing the vertical floating gate.

(Amended) A floating gate transistor, comprising: 14.

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first edge-defined vertical gate located above a first portion of the channel region and separated from the channel region by a first oxide thickness;

a second edge-defined vertical gate located above a second portion of the channel region and separated from the channel region by a second oxide thickness; and

a third edge-defined vertical gate located above a third portion of the channel region and separated from the channel region by the second oxide thickness.